IN THE SPECIFICATION

Please replace the following paragraphs:

Page 3, line 10 to page 3, line 20.

Accordingly, in ~~one~~ an embodiment, a method of controlling the impedance of a bus in an information handling system (IHS) is disclosed. The method includes providing a board on which a first bus is coupled to a first connector, the first bus exhibiting a bus impedance, the first connector exhibiting a connector impedance which is greater than the bus impedance. The method also includes providing a riser card situated in the first connector, the riser card including a second connector exhibiting an impedance approximately equal to the connector impedance of the first connector. The method further includes providing, on the riser card, an interconnect between the first and second connectors, the interconnect exhibiting an impedance sufficiently low to compensate the amount by which the connector impedance exceeds the bus impedance.

Page 3, line 22 to page 4, line 6.

In ~~another~~ an embodiment, an information handling system (IHS) is disclosed which includes a motherboard including a processor and a port which is situated on the motherboard and coupled to the processor. The IHS also includes a first connector situated on the motherboard and coupled to the port by a first bus therebetween, the first bus exhibiting a bus impedance, the first connector exhibiting a connector impedance greater than the bus impedance. The IHS further includes a riser card situated in the first connector, the riser card including a second connector and an interconnect between the second connector and the first connector, the second connector exhibiting a connector impedance approximately equal to the connector impedance of the first connector. The impedance of the interconnect is

selected to be sufficiently low to compensate the amount by which the connector impedance exceeds the bus impedance.

Page 4, line 8 to page 4, line 14.

In ~~another~~ an embodiment, the IHS further includes an expansion card situated in the second connector of the riser card, the expansion card including a second bus exhibiting a bus impedance approximately equal to the impedance of the first bus. The impedance of the interconnect is selected to be sufficiently low that the aggregate impedance of the first connector, the interconnect and the second connector is approximately the same as the first impedance. The second bus is an extension of the first bus.

Page 4, line 22.

FIG. 1 is a block diagram of an embodiment of an information handling system.

Page 5, line 5 to page 5, line 7.

FIG. 4 is a graph illustrating an embodiment of the uncompensated vs. the compensated complete return path loss showing the significant improvement achieved using the disclosed compensation technique.

Page 5, line 9 to page 5, line 11.

FIG. 5 is a graph illustrating an embodiment of the uncompensated vs. the compensated complete path attenuation further demonstrating the significant improvement achieved using the disclosed compensation technique.

Page 5, line 19 to page 5, line 21.

FIG. 1 is a block diagram of an information handling system 100 which experiences impedance discontinuity problems when two bus connectors are

situated in close proximity ~~of~~ to one another on a bus.

Page 8, line 2 to page 8, line 13.

A bus, such as a PCI or PCI-X bus 170, is situated on motherboard 200 using microstrip transmission line traces. While the bus is made of several such traces to form the address, data and control lines thereof, a representative microstrip transmission line trace 170' is shown in the perspective cross section view of FIG. 2B. ~~Since~~ Because bus 170 is a microstrip transmission line structure, a ground plane metallization 171 is situated on the side of board 200 opposite that on which trace 170' is situated. Returning to FIG. 2A, bus 170 extends from port 115A to bus connector 175. In this particular embodiment, bus connector 175 is a PCI or PCI-X bus connector. Other embodiments are contemplated wherein other bus structures and corresponding bus connectors are employed. Connector 175 includes a respective pin for each of the aforementioned address, data and control lines of bus 170.

Page 9, line 1 to page 9, line 8.

Expansion card 190 is situated in connector 180 in an orientation which is substantially perpendicular to riser card 180 and substantially parallel with motherboard 200. ~~Since~~ Because expansion card 190 is parallel with motherboard 200 rather than the more typical perpendicular orientation with respect to the motherboard, the vertical height of the IHS depicted in FIG. 2A is smaller than it would otherwise be. However, it has been found that in this approach, impedance discontinuities associated with connectors 175 and 180 are encountered because these connectors are so close to one another.

Page 10, line 9 to page 10, line 24.

In a vertically compact IHS such as that described above with a 1U height where the space for a riser card 180 is very limited, connectors 175 and 185 are

very close together, namely approximately 1 inch apart. Under these conditions, connectors 175 and 185 tend to exhibit a higher impedance than the microstrip transmission line traces which connect thereto. Connectors 175 and 185 exhibit an impedance of approximately 80 ohms whereas the microstrip transmission line traces exhibit an impedance of approximately 60 ohms in this particular example. ~~Since~~ Because connectors 175 and 185 are so closely spaced, rather than merely causing the IHS to suffer the adverse effects of two separate mismatched connectors, the two connectors effectively appear as one very large merged impedance discontinuity to the surrounding bus structure. This problem is solved in the IHS shown in FIG. 3A – 3C by using a lowered impedance interconnect to replace microstrip transmission line traces 187' of FIG. 2B to effectively lower and compensate for the high impedance of the large discontinuity to bring the overall aggregate impedance of the two connectors and the impedance interconnect closer to 60 ohms, or back to approximately 60 ohms, which is the impedance of bus 170.

Page 11, line 16 to page 12, line 2.

FIG. 4 is a graph of complete path return loss (RL) from port 115A which may be regarded as the signal source to port 192A which may be regarded as the signal load or termination point. Frequency in GHz is plotted along the x axis and return loss in dB is plotted on the y axis. The uncompensated return loss associated with the IHS of FIG. 2A – 2C is denoted by the curve marked with triangles. The compensated return loss associated with the IHS of FIG. 3A – 3C is denoted by the curve marked with diamonds. Return loss represents the amount of reflection observed from an interconnect system. Lower return loss, such as shown in the compensated case indicated by the diamonds, is indicative of a more closely matched load and diminished discontinuities. In FIG. 4, it is seen that there is significant improvement in the compensated case indicated by the curve with diamonds ~~since~~ because less incident signal is reflected back along the signal path from port 115A to port 192A.